

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 3-13 and 16-20 are pending in the present application. Claims 3, 9, 13, 16 and 19 are amended and Claims 1, 2, 14 and 15 are canceled by the present amendment.

In the outstanding Office Action, Claims 1-13 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 4,484,273 to Stiffler et al. (herein "Stiffler") in view of U.S. Patent No. 6,243,808 to Wang; and Claim 14 was rejected under 35 U.S.C. § 103(a) as unpatentable over Stiffler in view of Wang and U.S. Patent No. 5,148,161 to Sako et al. (herein "Sako").

Applicant respectfully traverses the rejection of Claims 1-13 under 35 U.S.C. § 103(a) as unpatentable over Stiffler and Wang.

Claim 3 is amended to be in independent form, to more clearly recite the features of the invention, and to recite features of Claims 1 and 2, which are canceled. In particular, Claim 3 is directed to a microprocessor that includes, in part, a processor core, a memory management unit, and a bus interface. The memory management unit includes, in part, a pre-routing storing unit configured to store pre-routing information that indicates the connection state of signals of a switching circuit, and an address translation buffer configured to store virtual tag information for translating virtual addresses generated inside the processor into physical addresses. Each of the virtual tag information is stored by an entry and corresponds to bus switch control information for controlling a connection relationship of a bus switch. The bus interface is coupled to the processor core and the memory management unit and is configured to rearrange the bits of data transferred from the processor core. The bus interface includes, in part, a switching circuit coupled to a data input/output unit. The switching circuit is configured to receive the data to change the order of bits of the data according to the pre-

routing information. Further, the bus switch is configured, in part, to receive the data and change the order of bits per a predetermined number of the bits according to the bus switch control information corresponding to an entry in the address translation buffer. Independent Claim 16 includes similar features directed to a video/sound processing system.

In a non-limiting embodiment, Applicant's Figure 2 is a block diagram of a microprocessor 121 including a processor core 122, a memory management unit 123 and an external bus interface unit 124 connected to an external memory and including a data bus shuffle mechanism. When data is sent from the processor core 122 to the external memory the data bits may be shuffled, for example to encrypt the data to reduce the possibility of extraction of secret information in the data when the data appears on the external data bus.

The bus interface unit 124 includes a pre-router 129 that may change the order of the data bits based on information in a pre-router register 131 and a table lookaside buffer (TLB) 132 (e.g., pre-routing storing unit) in the memory management unit 123. Figure 8 shows a structure of an example of a table lookaside buffer (TLB) 132, which may act as an address conversion cache memory of the memory management unit. In this example, a section of the TLB that stores a set of information is called an entry. Virtual address tag information, for comparing with a virtual address, may be stored in each entry. If the content of a virtual address and a virtual address tag match, the translation reference information of the matching entry may be used to generate a physical address. Each entry of the TLB may include a bus switch control information storage unit (BSCID) 143 so that the connection scheme of the switch can be changed on a per-page basis.

Moreover, as shown in Applicant's Fig. 8, each BSCID 143 (e.g., each of the bus switch control information) corresponds to a virtual address tag (VATAG) 141 (e.g., virtual tag information) of the entry. For example, Applicant's Fig. 7 is a table showing the correspondence between the bus switch connection schemes (i.e., "BUS SWITCH") and the

bus switch control information parameters (i.e., "BUS SWITCH CONTROL). In the table, each row shows a connection scheme that corresponds to a particular bus switch control information. The entries in the A column of the bus switch connection scheme section indicate which signal of the external bus (e.g., E, F, G or H) is connected to the A signal of the internal bus (pre-router), when particular bus switch control information is issued. Columns B, C and D indicate similar information for those internal signals. For example, when bus switch control information 0x00 is issued, internal signal A is connected to external signal E, internal signal B is connected to external signal F, internal signal C is connected to external signal G, and internal signal D is connected to external signal H.

Applicant respectfully submits that Stiffler and Wang, whether taken individually or in combination, fail to teach or suggest each feature of the claimed invention. As noted in the Office Action, Stiffler fails to teach a bus interface configured to rearrange the bits of the data transferred to and from the processor core. Wang describes a processor function that swaps bits, bytes and words. In Fig. 1 of Wang, an apparatus for performing bit swapping includes a matrix of signal path selection means arranged in rows. Wang indicates that a common control signal (signals C(1)-C(3)) controls each row such that it either passes all "non-swapped" bit values on the first input of each selection means or passes all "swapped" bit values on the second input of each selection means. For instance, in the case of row 1 of Fig. 1, Wang indicates that when the control signal is in a first state, each of the first input bit values b(0)-b(7) are passed through a corresponding selection means s(0)-s(7), based on the first state of the control signal. In other words, if control signal C1 indicates "swap," each signal pair (e.g., b(0)/b(1), b(2)/b(3), etc...) is swapped. Thus, Wang describes a system having a common control signal that indicates "non-swap" or "swap" using a single binary bit to perform a symmetrical rearrangement of bits.¹

¹ Wang at column 4, lines 8-26, and column 5, lines 13-15.

On the other hand, Wang and Stiffler are completely silent regarding any pre-routing storing unit that stores any information indicating the connection state of signals of the switching circuit. Further, Wang and Stiffler fail to teach or suggest storage of virtual tag information for translating virtual addresses into physical addresses, and fail to teach or suggest virtual tag information that is stored by entries that correspond to bus switch control information for controlling bus switch connection relationships.

Accordingly, Applicant respectfully submits that independent Claims 3 and 16, and claims depending therefrom, patentably define over Stiffler and Wang, whether taken individually or in combination.

Further, regarding Claims 5, 7, 8 and 10-13, Applicants respectfully traverse the assertion in the Office Action that “routing tables that control routing switches are well known.”² Amended independent Claim 1 requires an address translation buffer that stores virtual tag information for translating virtual addresses generated inside the processor into physical addresses. Each of the virtual tag information is stored by an entry and corresponds to bus switch control information for controlling a connection relationship of a bus switch. However, as discussed above, Stiffler and Wang fail to teach or suggest that feature. In addition, Stiffler and Wang fail to teach or suggest that bus switch control information is stored by the memory management unit, as recited in Claim 8, and Stiffler and Wang fail to teach or suggest that the memory management unit stores the bus switch control information in each entry of the address translation cache memory, as recited in Claim 10.

Accordingly, Claims 5, 7, 8 and 10-13 are believed to patentably define over Stiffler and Wang for those reasons in addition to the reasons discussed above with respect to independent Claims 3 and 16.

² Office Action at page 3, lines 8-13.

In addition, Applicant respectfully traverses the rejection of Claim 14 under 35 U.S.C. § 103(a) as unpatentable over Stiffler in view of Wang and Sako.

Amended Claim 16 includes features of canceled Claims 14 and 15. Claim 16 is believed to patentably define over Stiffler and Wang as discussed above, and Applicant respectfully submits that Sako also does not teach or suggest claimed features lacking in the disclosures of Stiffler and Wang. In particular, Applicant notes that Sako merely indicates that an input bit exchanger 614 (see Sako Fig. 8) rearranges bits so that input floating point data is aligned with a floating point format of a DSP. Further, Sako indicates that an output bit exchanger 624 rearranges the bit arrangement stored in the buffer register 620 to provide an arrangement which is the reverse of that provided by the input bit exchanger 614. Thus, these bit exchangers merely rearrange bits that are internal to a DSP, for compatibility with the DSP, and do not rearrange bits for encrypting data that appears on an external bus of the DSP.³ In other words, Sako does not indicate that any data external to the DSP is rearranged (i.e., the rearrangement is only apparent internal to the DSP). Therefore, Sako also does not teach or suggest a memory configured to hold rearranged content from the microprocessor, as required by Claim 16.

In addition, Applicant respectfully traverses the assertion in the Office Action that “[i]t would have been obvious to include the memory management and bit rearrangement structure in the video/audio system of Sako because this would have provided for fast bit conversion and memory control.”⁴ However, as discussed above, Sako merely describes a DSP that includes internal bit exchangers to make an external data format compatible with an internal format, and there is not even a suggestion in Sako or the other cited references to provide bit swapping of data that appears on external data buses. Thus, even if one of skill in the art were motivated “for fast bit conversion and memory control” they would not have

³ Sako at column 6, line 35, to column 7, line 29.

⁴ Office Action at page 4, lines 7-9.

been able to modify Sako to provide rearrangement of bits that appear on an external bus and that may be temporarily held in a memory coupled to the bridge, as required by Claim 16.

Thus, Applicant respectfully submits that independent Claim 16, and claims depending therefrom, also patentably define over Siffler, Wang and Sako, whether taken individually or in combination.

Accordingly, Applicant respectfully submits that independent Claims 3 and 16, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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